ABSTRACT OF THE DISCLOSURE

The present invention discloses a TFT array substrate that is fabricated using a four-mask process and a method of manufacturing that TFT array substrate. The gate line and gate electrode of the array substrate is surrounded by the metallic oxide after finishing a first mask process using thermal treatment. As a result, the gate line and gate electrode are not eroded and damaged by the etchant and stripper during a fourth mask process. Further, buffering layer can optionally be formed between the substrate and the gate line and gate electrode. Thus, silicon ions and oxygen ions included in the substrate are not diffused into the gate line and electrode. Accordingly, the line defect such as a line open of the gate line and gate electrode is prevented, thereby preventing inferior goods while increasing the manufacturing yield.